REMARKS/ARGUMENTS

1. Objection to the claims:

Claims 1, 6-8, 14, 15, 17, 20, and 21 are objected to due to informalities. These claims contain the phrases "first power" and "second power". It appears these should be "first power source" and "second power source". Appropriate correction is required.

Response:

The claims have been amended to correct these informalities. The phrases "first power" and "second power" now read "first outer power pin" and "second outer power pin", respectively. Acceptance of the corrected claims is respectfully requested.

2. Rejection of claims 1-7 and 20 under 35 U.S.C. 102(b):

Claims 1-7 and 20 are rejected under 35 U.S.C. 102(b) as being anticipated by Savelli (US 6,133,777).

Response:

Claims 1-7 and 20 have been cancelled, and are no longer in need of consideration.

3. Rejection of claims 8, 10-16, and 21 under 35 U.S.C. 103(a):

Claims 8, 10-16, and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Savelli (US 6,133,777) in view of Seki (US 5,122,692).

Response:

Claim 8 has been amended to distinguish from the prior art combination of Savelli and Seki and to clarify the claim language. Notably, claim 8 now recites that "a gate of the first transistor is directly connected to the second outer power pin without additional circuits or transistors" and that "a gate of the second transistor is directly connected to the first outer power pin without additional

circuits or transistors".

According to Savelli's figure and patent claims 1, 7, and 12, the first terminals of transistors 3 and 4 are connected to external power sources via two level-shifters, and these two level-shifters are controlled by a control signal. Furthermore, only one external power source is connected to the first terminals of transistors 3 and 4, with the other power source being V_{SS}, and the output voltage is controlled by control signal.

In the instant application, on the other hand, the first terminals and gates of the first and second transistors are directly connected to outer power pins without the need for additional circuits or transistors. This means that the outer power pins are directly connected to the first terminals and gates of first and second transistors at the same time. One outer power pin is V_{PP} and the other is V_{DD}, and V_{SS} is not used as an outer power pin. Furthermore, the intermediate voltage is generated automatically with no additional control signal being required, as is the case with Savelli's teachings.

For these reasons, the applicant respectfully submits that the combination of Savelli and Seki fails to teach all of the limitations contained in the currently amended claim 8, and claim 8 should be allowable over the cited prior art. Claims 10-16 and 21 are dependent on claim 8, and should be allowed if claim 8 is allowed. Reconsideration of claims 8, 10-16, and 21 is therefore respectfully requested.

4. Rejection of claims 17-19 under 35 U.S.C. 103(a):

Claims 17-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Savelli (US 6,133,777) in view of Seki (US 5,122,692).

Response:

Claims 17-19 are dependent on claim 8, and should be allowed if claim 8 is allowed. Reconsideration of claims 17-19 is therefore respectfully requested.

In view of the claim amendments and the above arguments in favor of patentability, the applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Sincerely yours,

Winston Hsu Date: 12/21/2006

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